

FIG. 1A (PRIOR ART)

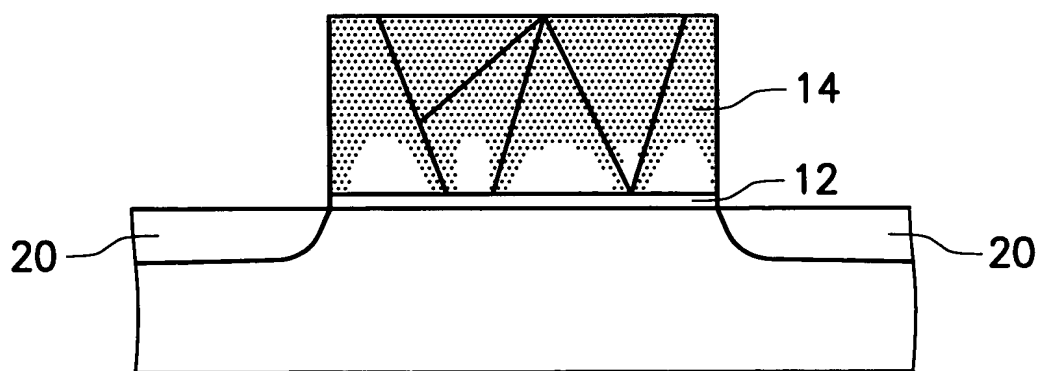


FIG. 1B (PRIOR ART)

A cross-sectional view of a semiconductor device. A substrate 20 is shown with a recessed region. A layer 12 is formed on the surface of the substrate 20. A patterned layer 14 is formed on top of layer 12, featuring a series of parallel, slanted lines. The layer 14 is shown with a stippled texture.

A cross-sectional view of a semiconductor device. A substrate 20 is shown at the bottom. A layer 12 is formed on the substrate. A patterned layer 14 is formed on the layer 12, featuring a series of triangular or V-shaped structures with a dotted texture.

FIG. 2 (PRIOR ART)

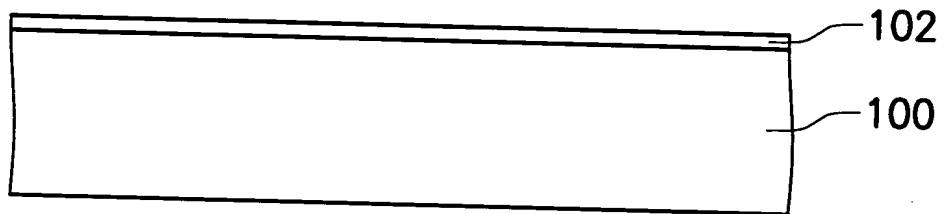


FIG. 3A

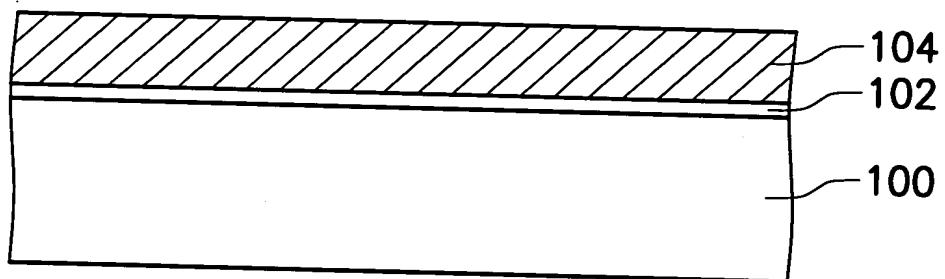


FIG. 3B

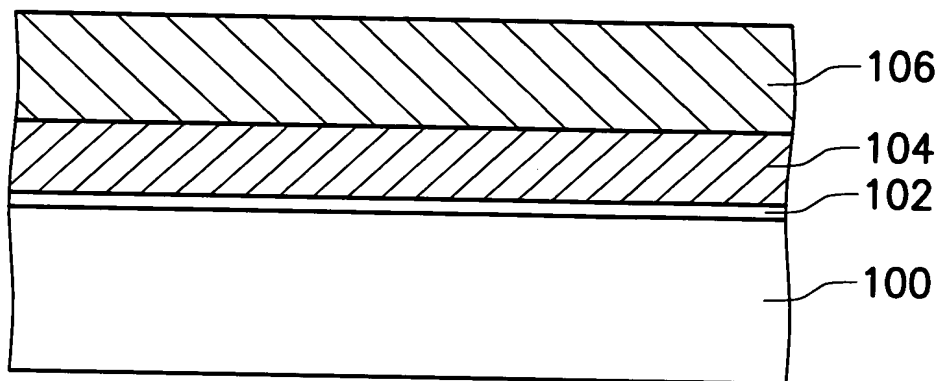


FIG. 3C

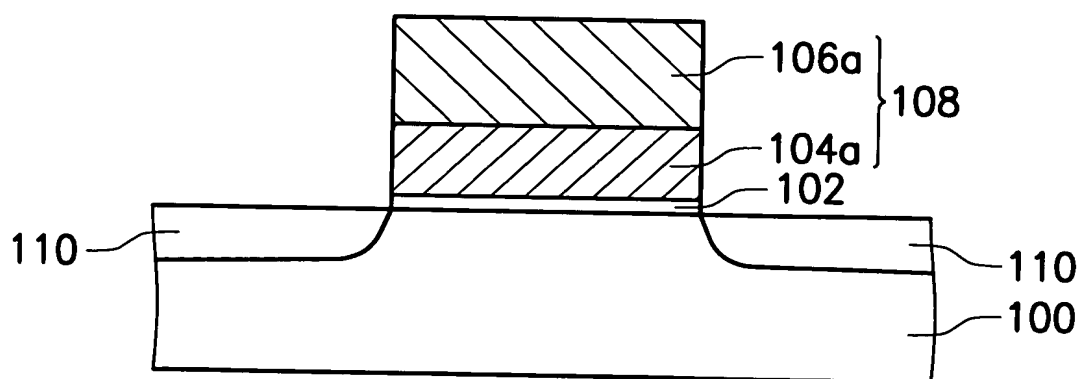


FIG. 3D